IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Chang Seo Park et al.	Docket No.:	061472-0308425
Serial No.:	10/826,665	Group Art Unit:	2813
Filing Date:	April 16, 2004	Examiner:	Harrison, Monica D.
For:	**A METHOD TO FABRICATE CMOS DEVICE WITH DUAL METAL GATE ELECTRODES**		

OFFICE ACTION RESPONSE

MAIL STOP AMENDMENT
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This paper is filed in response to the Office Action dated March 22, 2006.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 5 of this paper.

CLAIMS

1. (Currently amended) A method of fabricating a CMOS device comprising the steps of:

(a) forming a gate dielectric on a semiconductor substrate that can be sectioned into a p-well region for forming an NMOSFET and a n-well region for creating PMOSFET;

(b) forming [[a]] an aluminum nitride buffer layer material over the gate dielectric;

(c) depositing a first metal on the buffer layer;

(d) selectively etching the first metal with a first etchant so that the buffer layer is exposed on one of said p-well and n-well regions;

(e) depositing a second metal on both the exposed buffer layer and the remaining first metal;

(f) removing said first metal and said second metal and said buffer layer in selected areas so as to form a PMOSFET gate electrode and an NMOSFET gate electrode of said CMOS device; and

(g) annealing remaining portions of said first metal and said second metal and said buffer layer to consume said portions of said buffer layer by reacting with said first metal and said second metal to form first and second conductive alloys with first and second work functions respectively.

2. (Original) A method as recited in claim 1 wherein said buffer layer material is selected to have a resistance to said first etchant for protecting said gate dielectric from said first etchant.

3. (Cancelled)

4. (Currently amended) A method as recited in claim [[3]] 1 wherein said buffer layer has a buffer layer thickness less than 20nm.

5. (Original) A method as recited in claim 1 wherein said first etchant is a wet chemical solution including a mixture of sulfuric acid and hydrogen peroxide.

6. (Original) A method as recited in claim 1 wherein said first etchant is a wet chemical solution including a mixture of hydrofluoric acid and hydrogen peroxide.

7. (Original) A method as recited in claim 1 wherein said annealing is done at a temperature in excess of 400°C.

8. (Original) A method as recited in claim 1 wherein said first metal is hafnium and said second metal is tantalum.

9. (Original) A method as recited in claim 1 wherein said forming a buffer layer material includes a process selected from the group consisting of physical vapor deposition (PVD), chemical vapor deposition (CVD) and atomic layer deposition (ALD).

10. (Currently amended) A method as recited in claim [[3]] 1 wherein a composition ratio of ~~said aluminum to said nitrogen~~ the aluminum nitride is selected to achieve desired work functions of said metal alloys.

11. (Currently amended) A method of determining a work function of a metal gate electrode comprising:

determining a desired work function of a metal gate electrode including

(a) depositing [[a]] an aluminum nitride buffer layer material on a gate dielectric;

(b) depositing a metal on said buffer layer material; and

(c) annealing said buffer layer and said metal to cause said buffer material and said metal to react and form an alloy having the desired work function.

12. (Cancelled)

13. (Currently amended) A method as recited in claim ~~12~~ 11 wherein a composition ratio of ~~said aluminum and said nitrogen~~ the aluminum nitride is selected to achieve a desired said work function.

14. (Currently amended) A method as recited in claim [[3]] 1 wherein the first metal and second metal are selected from the group consisting of titanium (Ti), hafnium (Hf) and tantalum (Ta).

15. (Currently amended) A method as recited in claim [[3]] 1 wherein the first metal and second metal have an electronegativity of less than 1.34 ~~Ev~~.

16. (Currently amended) A metal gate for CMOS applications, wherein the contact area between said metal gate and adjacent metal gate dielectric is comprised of an alloy formed from ~~AlN_x~~ aluminum nitride and a metal whose electronegativity is less than 1.4.

17. (Original) A metal gate as in Claim 16, where the metal is Hf, and the alloy has a work function of approximately 4.4Ev, appropriate for NMOS.

18. (Original) A metal gate as in Claim 16, where the metal is Ta, and the alloy has a work function of approximately 4.9Ev, appropriate for PMOS.

REMARKS

Section 102 Rejections

The Office Action rejects claims 1, 2 and 11 under 35 U.S.C. 102(b) as anticipated by Wu. Applicants traverse this rejection for the following reasons. Wu's invention does not describe the method of the present application as now claimed, where a buffer layer is deposited prior to the deposition of metal forming metal gate electrodes, and the buffer layer is selected to be consumed by reaction with the metal in an annealing process, as described in amended claim 1. In regard to claim 11, Wu does not describe a buffer layer that, when subjected to annealing, reacts with a metal to provide a desired work function.

The Office Action refers to Fig. 1, reference 8, of Wu as a buffer layer. The layer 8 of Fig. 1 referred to by the Office Action is not the buffer layer as described by claims 1, 2 and 11 of the present application, which according to claims 1 and 11 reacts with metal to form a gate electrode. In contrast, Wu's layer 8 of Fig. 1 is completely removed, as described by Wu at col. 4, lines 49 – 50. The Office Action also refers to Fig. 6, reference 16, of Wu as a metal. The polysilicon layer 16 of Wu is not a metal as described in claims 1 and 11. Wu therefore does not teach or suggest the buffer layer of claims 1 and 11, and also does not teach or suggest the buffer layer of claims 1 and 11 being consumed by a metal layer.

In further description of the difference between Wu's invention and that of amended claims 1 and 11 of the present application, the invention described by Wu focuses on nitridation of gate oxide using LPD (liquid phase deposition). The formed nitride is silicon oxynitride (SiON), which is different from the aluminum nitride buffer layer of the present application as now claimed, which upon annealing reacts with a metal and becomes a gate electrode. The nitride used in Wu's invention is used as a gate dielectric, and is not a gate electrode. Thus, the buffer layer of claims 1 and 11 (which becomes a gate electrode upon

annealing) serves a very different function than the gate dielectric of Wu. Wu's invention does not include the metal alloy gate of claims 1 and 11 of the present application, and Wu does not describe how to form a specific metal alloy gate with a desired work function for a dual metal gate integration, as in amended claims 1 and 11, which upon annealing reacts with a metal and becomes a gate electrode.

With regard to claim 2, the Office Action refers to Fig. 1, reference 8, of Wu as a buffer layer. As explained above, the layer 8 of Wu does not serve the function of the buffer layer of claims 1, 2 and 11. Wu's layer 8 is completely removed (see Wu at col, 4, lines 49 – 50), and therefore can not be the buffer layer of claims 1, 2 and 11, which layer reacts with the metal, being consumed (not removed) by an annealing process. Applicant therefore believes claim 2 is novel and allowable.

In specific response to the Office Action comments regarding claim 11, the Office Action refers to Wu's Fig. 1, reference 8, as a buffer layer. As explained above, this layer 8 is removed (col. 4, lines 49 – 50). The Office Action refers to Wu's Fig. 6, reference 16, as a metal, but reference 16 is polysilicon, which is not a metal as described in claims 1, 2 or 11 according to the present application. The Office Action refers to Wu, at col. 2, lines 37 – 54, as describing the annealing process of claims 1 and 11. Wu's anneal (col. 2, lines 51 – 54) is used to "condense LPD-oxide," which is not the annealing process described in claims 1 and 11 of the present application, which causes the buffer layer to react and be consumed with a metal layer.

Section 103 Rejections

The Office Action rejects claims 4 – 7 , 9, 10, and 13 under 35 U.S.C. 103(a) as unpatentable over Wu in view of Lim. Applicants traverse this rejection for the following reasons. Claims 4 – 7, 9, 10, and 13 depend on claims 1 or 11, which as explained above are

believed to be allowable. Applicants therefore believe claims 4 - 7, 9, 10, and 13 are allowable as they add further limitation to allowable claims. In addition, Applicants respond to the Office Action in more detail as follows. The Office Action points to Lim at col. 2, lines 46 – 60, where Lim describes the use of aluminum nitride as a trench liner. Applicants point out that a trench is a structure used to isolate adjacent independent devices, and is a very different use and unrelated to the use of aluminum nitride in the present application as a buffer layer under the deposition of a metal gate electrode, where the metal layers are selected to react to consume the buffer layer. Therefore, Lim's use of aluminum nitride can not be combined with Wu to teach or suggest the claims of the present application.

The Office Action rejects claims 8, 14 and 15 under 35 U.S.C. 103(a) as unpatentable over Wu and Lim in view of Huotari. Applicants traverse this rejection for the following reasons. Wu does not provide a buffer layer below a metal layer that combines/reacts with a metal layer to consume the buffer layer as in claim 1, upon which 8, 14 and 15 depend. Lim deals with the unrelated subject matter of a trench for isolation of devices, and Lim's use of aluminum nitride in a trench can therefore not be combined with Wu to teach or suggest the aluminum nitride buffer of claim 1. In addition, Huotari does not disclose a buffer layer that reacts and is consumed with a metal to form a gate electrode, and the discussion of gate electrodes therein reveals nothing that can be combined with Wu and Lim to suggest the present claims 8, 14 or 15. Applicants therefore believe these claims are allowable.

Regarding the Office Action rejection of claims 16, 17 and 18, Huotari does not describe a contact area between a metal gate and an adjacent metal gate dielectric comprised of an alloy formed from AlN_x and a metal whose electronegativity is less than 1.4. Huotari therefore does not teach or suggest the invention of claims 16, 17 or 18. In view of the above discussion, Applicants believe these claims are allowable.

CONCLUSION

Applicant has explained the differences between the claims and the cited references, and believes the claims are now in condition for allowance.

If any further questions should arise prior to a Notice of Allowance, the Examiner is invited to contact the attorney at the number set forth below.

Date: July 24, 2006

Respectfully submitted

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